In the Claims

Please cancel claims 4, 5 and 9.

Please amend claims 1-3, 6-8 and 9-14 as follows.

1. (currently amended) A method of fabricating a buried heterostructure semiconductor device, comprising:

producing a hybrid current confinement region adjacent to an active ~~layers~~ layer of the device, by:

disposing in a selected sequence ~~of the p-n-p layers surrounding~~ adjacent to selected surface portions of the active layer, a layer of first material doped with a first dopant and a layer of second material doped with a second dopant; and

disposing a semi-insulating material ~~around~~ adjacent to the ~~p-n-p~~ layers of the first and second materials ~~surrounding the active layers~~; and

disposing a layer of dielectric material directly on the semi-insulating material, wherein the arrangement of the disposed materials produces the hybrid current confinement region during fabrication of the buried heterostructure semiconductor device.

2. (currently amended) The method of claim 1, wherein the semiconductor device is a buried heterostructure laser.

3. (currently amended) The method of claim 1, wherein the semi-insulating material ~~is~~ comprises InP ~~doped with Fe~~ to provide current confinement for current generated in the active layer.

4. (canceled)

5. (canceled)

6. (currently amended) The method of claim 1, ~~5 wherein producing further comprises~~ further comprising a step of:

depositing a ~~doped p-type~~ capping layer over ~~the~~ a first mesa to ~~provide~~ form a ~~the n-p-n-p~~ current blocking structure, wherein the first mesa supporting the active layer.

7. (currently amended) The method of claim 6, further comprising a step of ~~wherein producing further comprises~~:

etching ~~away~~ portions of the current blocking structure ~~using a wide oxide mask disposed over the capping layer~~ to form a second mesa covering the first mesa.

8. (currently amended) The method of claim ~~5~~ 7, further comprising a step of ~~wherein producing further comprises~~:

~~re-growing~~ forming a semi-insulating material over the etched ~~n-p-n-p~~ blocking structure.

9. (canceled)

10. (currently amended) A semiconductor device comprising:

a ~~semiconductor~~ substrate supporting an active layer~~region comprised of a multiple quantum well active regions and confinement layers having defined gratings and grating overgrowth regions to produce a laser device~~; and

a current confinement layer comprising:

~~a sequence of doped n-p-n-p~~ first and second semiconductor layers adjacent to selected wall surfaces of the active ~~region~~ layer to produce a ~~n-p-n-p~~ blocking structure, wherein the first and second layers are doped with first and second dopants, respectively; ~~and~~

a semi-insulating semiconductor material adjacent to the ~~p-n~~ blocking structure; and

a dielectric layer disposed directly on the semi-insulating material.

11. (currently amended) The semiconductor device of claim 10 further comprising:

a heavily doped contact layer disposed over the active layer.

12. (currently amended) The semiconductor device of claim 10 wherein the semi-insulating material ~~is Fe doped~~ comprises InP.

13. (currently amended) The semiconductor device of claim 10 wherein the semiconductor substrate material ~~is n-type doped~~ comprises InP.

14. (currently amended) The semiconductor device of claim ~~10~~11 wherein the contact ~~material~~layer ~~is~~ comprises p-type InGaAs.

Please add claims 15-27 as follows.

15. (new) The method of claim 1 further comprising:

depositing a contact layer over the first and second layers.

16. (new) The method of claim 15 further comprising:

forming a contact electrode directly on the contact layer, the semi-insulating material and the dielectric layer.

17. (new) The method of claim 3, wherein the semi-insulating material is doped with Fe.

18. (new) The method of claim 1, wherein at least one of the first and second materials directly contacts the selected surface portions of the active layer.

19. (new) The method of claim 1, wherein the first and second dopants include p-type and n-type dopants, respectively.

20. (new) The method of claim 1, wherein the first and second dopants include n-type and p-type dopants, respectively.

21. (new) The semiconductor device of claim 10 further comprising:

a heavily doped contact layer disposed over the blocking structure.

22. (new) The semiconductor device of claim 21 further comprising:

a contact electrode provided directly on the contact layer, the semi-insulating material and the dielectric layer.

23. (new) The semiconductor device of claim 10, wherein the first and second dopants include p-type and n-type dopants, respectively.

24. (new) The semiconductor device of claim 10, wherein the first and second dopants include n-type and p-type dopants, respectively.

25. (new) The semiconductor device of claim 10, wherein the blocking structure includes a p-n blocking structure.

26. (new) The semiconductor device of claim 12, wherein the semi-insulating material is doped with Fe.

27. (new) The semiconductor device of claim 13, wherein the semiconductor substrate material is doped with an n-type dopant.

In the Figures:

Applicants amend Figure 2 to change "21 current blocking structure" to --21 first two layers of current blocking structure--. A replacement drawing sheet showing the amended figures, which includes the desired changes without markings, is attached herewith. The replacement drawing sheet includes the identifier "Replacement Sheet".